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APPROACHES TO DESIGN & IMPLEMENT HIGH SPEED-LOW POWER DIGITAL FILTER: REVIEW

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Abstract

Digital Filters are important elements of Digital Signal Processing (DSP) systems. Digital Filters can be realized by various Digital Filter Structures like Direct Form-I, Direct Form-II, Cascade, Parallel,T ransposed structures etc.These structures provide a space for selection of appropriate structure for reduction of power consumption and improvement in speed of Digital filters which is significantly important for all high-performance DSP applications. Major factors influencing the choice of specific realization are computational complexity, memory requirements and finite word length effects. The techniques which are used to achieve low power consumption in VLSI-DSP applications span a wide range, from algorithm and architectural levels to logic, circuits and device levels. Pipelining and parallel processing can be used to reduce power consumption by reducing supply voltage. Power consumption can be reduced by reducing effective capacitance which can be achieved by reducing the number of gates or by algorithmic strength reduction where the number of operations in an algorithm is reduced. Power can also be reduced by reducing memory access. This paper reviews several techniques and approaches used by previous authors for designing & implementing low power-high speed digital filters.

Keywords

High speed, Low power, Multiplier-Accumulator (MAC), multiplier free, Pipelining.

I. **Introduction**

The developments in electronic technology are taking place at a tremendous speed. Recently, Digital Signal Processing (DSP) is used in numerous applications such as video compression, digital set-top box, cable modems, digital versatile disk, portable video systems/computers, digital audio, multimedia and wireless communications, digital radio, digital

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still and network cameras, speech processing, transmission systems, radar imaging, acoustic beam formers, global positioning systems, and biomedical signal processing. The field of DSP has always been driven by the advances in DSP applications and in scaled very-large-scale-integrated (VLSI) technologies. Therefore, at any given time, DSP applications impose several challenges on the implementations of the DSP systems. These implementations must satisfy the enforced sampling rate constraints of the real-time DSP applications and must require less space and power consumption.

DSP computation is different from general-purpose computation in the sense that the DSP programs are non terminating programs. In DSP computation, the same program is executed repetitively on an infinite time series. The non terminating nature can be exploited to design more efficient DSP systems by exploiting the dependency of tasks both within iteration and among multiple iterations. Furthermore, long critical paths in DSP algorithms limit the performance of DSP systems. These algorithms need to be transformed for design of high-speed or low-power implementations. The techniques which are used to achieve low power consumption in VLSI-DSP applications span a wide range, from algorithm and architectural levels to logic, circuits and device levels [1-2].Digital filters are essential elements of DSP systems. Digital filters are classified into two categories as: Finite Impulse Response (FIR) filter and Infinite Impulse Response (IIR) filter. Though FIR filters have linear phase property, low coefficient sensitivity and stability compare to IIR filter they consume more power than IIR filter in general. Strength reduction transformations are applied to reduce the number of multiplications in finite impulse response (FIR) digital filters.

There is a tremendous development in Integrated Circuit(IC) technology in last few years. Every couple of years advances in the state of the art led to higher performance, lower power dissipation, lower cost and greater density. We can no longer expect performance to naturally

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increase as a result of advances in IC technology, nor can we expect power dissipation to decrease as a function of the advances. In fact, one could argue that advances in clock speeds fell off the curve over a decade ago. In the same vein, power dissipation began falling off the pace about five years ago. The result is that we need to find new ways to satisfy our continuing demand for more performance, and new ways to achieve that performance at a lower power level. One way we can do this is by understanding how performance and power dissipation depend on other variables under our control.

There have been consistent efforts being taken to reduce power consumption since last few decades. Power consumption can be reduced by a combination of several techniques. Pipelining and parallel processing can be used to reduce power consumption by reducing supply voltage. Power consumption can be reduced by reducing effective capacitance which can be achieved by reducing the number of gates or by algorithmic strength reduction where the number of operations in an algorithm is reduced. Power can also be reduced by reducing memory access. The single most effective means to power-consumption reduction is clock gating where all functional units which need not compute any useful outputs are switched off by using gated clocks. Use of multiple-supply voltages and a simultaneous reduction of threshold and supply voltages are also effective in reducing power consumption. Most power-reduction approaches apply to dedicated, Programmable or Field Programmable Gate Array (FPGA) systems in a dual manner [1-2].Optimizations of the speed and power consumption of digital filters can be achieved by using dedicated operators instead of general ones whenever possible. Multiply and Accumulate (MAC) is an important unit of DSP systems. It decides the power consumption and speed of operation of DSP systems.

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II.TECHNIQUES OF POWER MINIMIZATION & SPEED IMPROVEMENT IN DIGITAL FILTERS

A. Pipelining and parallel processing

Pipelining transformation leads to a reduction in the critical path, which can be exploited to either increase the clock speed or sample speed or to reduce power consumption at same speed. Critical path is defined as the path with longest computation time among all the paths that contain zero delays, and the computation time of the critical path is the lower bound on the clock period of the circuit. In parallel processing, multiple outputs are computed in parallel in a clock period. Therefore the effective sampling speed is increased by the level of parallelism. Similar to the pipelining, parallel processing can also be used for reduction of power consumption. Pipelining reduces the effective critical path by introducing pipelining latches along the datapath.The power consumption of the pipelined filter is given by $P_{pip}=C_{total}\ \beta^2\ V_0 f$. Where C_{total} is total capacitance of the circuit, V0-supply voltage, f-clock frequency, β-power consumption reduction factor.Parallel processing can reduce power consumption of a system by allowing the supply voltage to be reduced.Power consumption of L-parallel system can be computed as: $P_{par} = \beta^2 C_{charge}\ V_0{}^2 f$, Where C_{charge} –charging capacitor along critical path Since maintaining the same sample rate, clock period is increased to LTseq.Where Tseq =1/f .This means that C_{charge} is charged in LT_{seq}, and the power supply can be reduced to βV_0.The supply voltage cannot be lowered indefinitely by applying more & more levels of pipelining and parallelism[3]**.** Cascade and parallel stuctures for Digital Filter are developed on the same concept.

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B. Unfolding

It is transformation technique that can be applied to a DSP program to create a new paradigm describing more than one iteration of the original program. More specifically, unfolding a DSP program by the unfolding factor *J* creates a new program that describes *J* consecutive iterations of the original program. Unfolding allows the DSP program to be implemented with an iteration period equal to iteration bound[B1]**.**If the basic iteration is unfolded J times the number of simultaneously processed samples increases linearly, while the critical path is not altered. Therefore the throughput increases at the rate J.So an arbitrary fast implementation can be achieved by using the appropriate number of unrolling [4].It can be applied to generate word parallel architectures that can be used for high speed & low power applications.

C. Retiming & Scheduling

Retiming is a transformation technique used to change the locations of delay elements in a circuit without affecting the input / output characteristics of the circuit. Retiming can be used to increase the clock rate of a circuit by reducing the computation time of the critical path. This technique is used to improve the throughput by moving registers in a circuit. The basic goal is to redistribute registers in the circuit to maximize throughput [5]. *Scheduling* consists of assigning execution times to the operations in a Data Flow Graph (DFG) such that the precedence constraints of the DFG are not violated. Retiming is considered to be a special case of scheduling. In bit-parallel scheduling, a DFG is statically scheduled to bit-parallel target architecture. The scheduling formulation is generally based on the folding equation. *Folding* is the process of executing several algorithm operations on a single hardware module and Scheduling is the process of determining at which time units a given algorithm operation is to be executed in hardware.

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III.APPROACHES TO REDUCTION IN COMPUTATIONAL COMPLEXITY FOR THE IMPLEMENTATION OF LOW POWER HIGH SPEED DIGITAL FILTER STRUCTURES

Computational complexity of Digital Filter structures is given by total number of multipliers and total number of two input adders required for it's implementation,which roughfly provides an indication of cost of implementation. Computational complexity of FIR Digital Filter structures is summarized in Table I.[6]

TABLE I. Computational complexity of various realizations of FIR filters of order N.

Structure	Number of Multipliers	Number of Two input adders
Direct Form	N+1	N
Cascade Form	N+1	N
Polyphase	N+1	N
Cascaded Lattice	2(N+1)	2N+1
Linear Phase	(N+2)/2	N

For the applications demanding low power and high speed Digital Filters ,the various approaches developed so far to reduce the number of multiplications and additions are discussed below:

1.Lefevre's modified approach for optimization of hardware multiplication by constant matrices

Strength reduction at algorithmic level can be used to reduce the number of additions and multiplications. Applications involving multiplication by constant are common in digital signal processing.A first solution proposed to optimize multiplication by constant was the use of the

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constant recoding, such as Booth's. This solution just avoids long strings of consecutive ones in the binary representation of the constant. Better solutions are based on the factorization of common subexpressions, simulated annealing, tree exploration, pattern search methods, etc In 2001, Lefe`vre proposed a new algorithm to efficiently multiply a variable integer by a given set of integer constants which was then modified by Nicolas Boullis and Arnaud Tisserand. A significant drop up to 40 percent in the total number of additions/subtractions is obtained by using this modified algorithm,[7].Strength reduction leads to a reduction in hardware complexity by exploiting substructure sharing.

2.**Subexpression elimination approach**

Numerical transformation techniques are used for reducing strength of DSP computations.These transformations rely upon subexpression elimination(also referred to as substructure sharing) to restructure the computation in such a manner that the performance in terms of speed, power and area of the computation can be improved. Subexpression elimination is applied to the multiple constant multiplication problem. Multiple constant multiplications are then extended to specific computations such as linear transformation and polynomial evaluation.The constant multiplications can be efficiently implemented in hardware by converting them into a sequence of additions and hardwired shifts. Such an implementation can be optimized by finding common subexpressions in the set of additions and shift operations [8].Optimization Using Rectangle Covering technique is used to find common subexpressions by transforming the problem as a rectangle covering problem. First, a set of all algebraic divisors of the polynomial expressions is generated and arranged in a matrix form, from which all possible common subexpressions, involving any number of variables can be detected. A heuristic rectangle covering algorithm is then used to iteratively find common subexpressions.The rectangle covering method is able to find multiple variable common

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subexpressions and produce better results than those produced by methods that can only find common subexpressions involving only a single variable at a time. But the algorithm suffers from two major drawbacks. The major drawback is that it is unable to detect common subexpressions that have their signs reversed. This is a major disadvantage, since when signed digit representations like CSD are used, a number of such opportunities are missed. Another disadvantage of this technique is that the problem of finding the best rectangle in the Kernel Intersection Matrix (KIM) is exponential in the number of rows/columns of the matrix. Therefore heuristic algorithms such as the ping-pong algorithm have to be used to find the best common subexpression in each iteration [9]. Multi-level logic synthesis techniques use a faster algorithm called Fast Extract (FX) for doing quick Boolean decomposition and factoring. This technique is much faster than the rectangular covering methods and produces results close to the most expensive routines using rectangle covering. This method is called as 2-term CSE method. The better results of the algorithm can be attributed to the fact that it can detect common subexpressions with reversed signs[10-11].

3. Approach to design Multiply and Accumulate (MAC) using Block Enabling Technique

Real-time signal processing requires high speed and high throughput Multiplier-Accumulator (MAC) unit that consumes low power, which is always a key to achieve a high performance digital signal processing system. A low power MAC unit can be designed and implemented using block enabling technique to save power. In any MAC unit, data flows from the input register to the output register through multiple stages such as, multiplier stage, adder stage and the accumulator stage. Within the multiplier stage, further, there are multiple stages of addition. During each operation of multiplication and addition, the blocks in the pipeline may not be required to be on or enabled until the actual data gets in from the previous stage. In block

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enabling technique, the delay of each stage is obtained. Every block gets enabled only after the expected delay. For the entire duration until the inputs are available, the successive blocks are disabled, thus saving power[12].

4. Computer Algebraic System approach

Conventional digital signal processing is based on numeric computations that might be unproductive to satisfy the needs of new efficient systems. Symbolic techniques can be used to complement traditional numeric algorithms. They can be used to efficiently search for new solutions, where a new low-sensitivity structure has been derived. Nowadays, computer programs enable knowledge about the design of algorithms, and can be used to employ that knowledge in symbolic manipulations. The use of computer algebra systems (CASs) and symbolic processing can help us gain insight into how some system works.The current leaders in implementing CASs (Mathematica by Wolfram Research and Symbolic Math Toolbox of MATLAB and Maple) are extremely powerful in doing symbolic mathematics for technical computing. They have demonstrated first, how a CAS can be used in examining the structure and performances of an existing digital filter; second, how to use the CAS in finding solutions for transforming an existing infinite impulse response (IIR) half-band filter to another digital filter that retains the passband/stopband performances of the start-up half-band filter, and third to use the CAS in order to develop a multiplierless IIR filter with an adjustable cutoff frequency. The multiplierless half-band IIR filters are useful for implementation using programmable logic devices such as FPGA with low-power consumption .Algebraic techniques are established in multi-level logic synthesis for the minimization of the number of literals and hence gates to implement Boolean logic[13-15].

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5. Approaches to reduce Algebraic operations

The problem of multiplying one data with several constant coefficients has been well studied over the years The computational complexity of VLSI digital filters using fixed point binary multiplier coefficients is normally dominated by the number of adders used in the implementation of the multipliers. It has been shown that using multiplier blocks to exploit redundancy across the coefficients results in significant reductions in complexity over methods using canonic signed-digit (CSD) representation, which in turn are less complex than standard binary representation[16]. A. G. Dempster and M. D. Macleod, in their paper titled "Use of minimum-adder multiplier blocks in FIR digital filters,"praposed three new algorithms for the design of multiplier blocks: an efficient modification to an existing algorithm, a new algorithm giving better results, and a hybrid of these two which trades off performance against computation time. Significant savings in filter implementation cost over existing techniques result in all three cases. For a given wordlength, it was found that a threshold set size exists above which the multiplier block is extremely likely to be optimal. In this region, design computation time is substantially reduced.

In the paper titled "Low-Complexity Constant Coefficient Matrix Multiplication Using a Minimum Spanning Tree Approach", Oscar Gustafsson, Henrik Ohlsson, and Lars Wanhammar proposed an algorithm for low complexity constant coefficient matrix multiplication based on differences. It uses a minimum spanning tree (MST) to select the coefficients, which warrants low execution time as an MST can be found in polynomial time [17-18].

In general, optimization techniques usually used for multiplierless filter design are complex, can require long run times, and provide no performance guarantees (Koter at al., 2003). Gordana Jovanovic Dolecek and Sanjit K. Mitra in their paper titled "Computationally Efficient Multiplier-Free Fir Filter Design", proposed simple efficient method for the design of multiplier-free FIR

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filters without optimization.The method uses the rounding to the nearest integer of the coefficients of the equiripple filter which satisfies the desired specification. Considering that the integer coefficient multiplications can be accomplished with only shift-and-add operations, the rounded impulse response filter is multiplier-free. The complexity of the rounded filter (the number of the sums and the number of integer multiplications) depends on the choice of the rounding constant. Higher values of the rounding constant lead to the less complexity of the rounded filter but also in a more distortion in the desired gain response. In the next step the sharpening technique is used to improve the magnitude characteristic and to satisfy the specification. In that way the overall filter is based on combining one simple filter with integer coefficients [19].

V.Conclusion

Low power high speed techniques for digital filter implementations are reviewed in this paper. Cascade and parallel structures may be used for Low power high speed Digital Filter Structures. Speed of Digital Filter can be improved by unfolding the various iterations of DSP program. A significant drop up to 40 percent in the total number of additions/subtractions is obtained by using Lefevre's modified approach for optimization of hardware multiplication by constant matrices. The ping-pong algorithm may be the best option to find the best common subexpression in each iteration.Designing MAC using block enabling technique results in low power consumption. Symbolic mathematics is extremely powerful tool for technical computing which reduces the computations thereby improving speed and optimizing power consumption. The method for the design of multiplier-free FIR filters without optimization technique has proven less complexity which results in high speed digital filter.

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