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SURVEY OF ONLINE HARDWARE TASK SCHEDULING AND PLACEMENT ALGORITHMS FOR PARTIALLY RECONFIGURABLE COMPUTING SYSTEMS

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ABSTRACT

Run time Partially Reconfigurable FPGAs find various applications in the field of Cryptography, Image processing, Network Security, Video streaming etc., because of low power consumption, high density, flexibility and high performance. Further more, the dynamism and true multitasking makes it popular in the area of today's advanced computing platforms. An powerful operating system is required to manage and sharing the resources among the various applications system is required. Out of several research issues in design of operating system of Reconfigurable devices, the on-line scheduling and placement of hardware tasks is non-polynomial problem. This paper deals with comprehensive survey of algorithms for on-line hardware task scheduling and placement in reconfigurable devices and their performance.

KEYWORDS

Computer aided design, Defragmentation, Dynamic reconfiguration, FPGA, on-line scheduling and placement, operating system, Run Time Partial reconfiguration, VLSI Design.

INTRODUCTION

Reprogrammable nature of FPGAs introduces new challenges and opportunities in design automation and still there is lack of developing CAD tools for synthesis and Compilation. The trend of utilizing reconfigurable FPGA's is drastically increasing due to high density, parallel computing nature, flexibility and low cost as compared to ASIC and general purpose processors. Katherine Compton, Scott Hauck [23] deals with complete introduction to reconfigurable computing system. Marco Platzner [28] deals with how the operating system approaches for dynamically reconfigurable hardware. The main function of resource management unit is online scheduling and placement of hardware tasks, developing algorithms for the same is an challenging issue. This paper is organised as follows: Section II deals with motivation, Section III deals with Run time Partial and Dynamic Reconfigurable FPGAs, Section IV Reconfiguration overhead, Section V deals with survey of scheduling, placement algorithms and defragmentation.

II.MOTIVATION

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In the field of Computer aided design automation, there is need of developing fast algorithms for partitioning, scheduling, protection, Placement, routing and communication . Andre Detlon and John Wawrzynek [4] discuss about the importance of Reconfigurable computing and its implications for design automation. Grant B.Wigley et al.[12] address the research issues in operating systems like partitioning, scheduling, placement and routing and its impact on system performance..

In developing online scheduling and placement algorithms, the main motivation is to reduce the factors like area fragmentation, reconfiguration overhead, reconfiguration latency and task rejection rates during scheduling and placement. The flow of VLSI circuit design in reconfigurable computing system is given in Figure.1

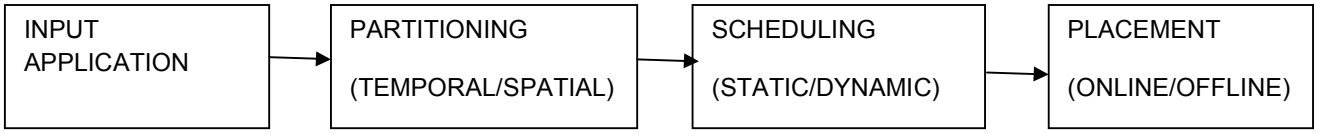

Figure.1 Flow of Operating Systems In Reconfigurable Computing Systems

III. RUN TIME PARTIAL AND DYNAMIC RECONFIGURABLE FPGA's.

Field Programmable Gate array consists of array of programmable logic blocks and its interconnections. The functionality of logic blocks and its interconnections are user programmable. The application that is loaded into FPGA constitutes various circuits which occupies group of logic blocks in FPGA. With the help of bitstream file from internal configuration memory, the logic blocks are identified for corresponding circuit of an application and the FPGA is configured by loading the bit stream. Figure.2 shows how application is configured in FPGA Architecture.

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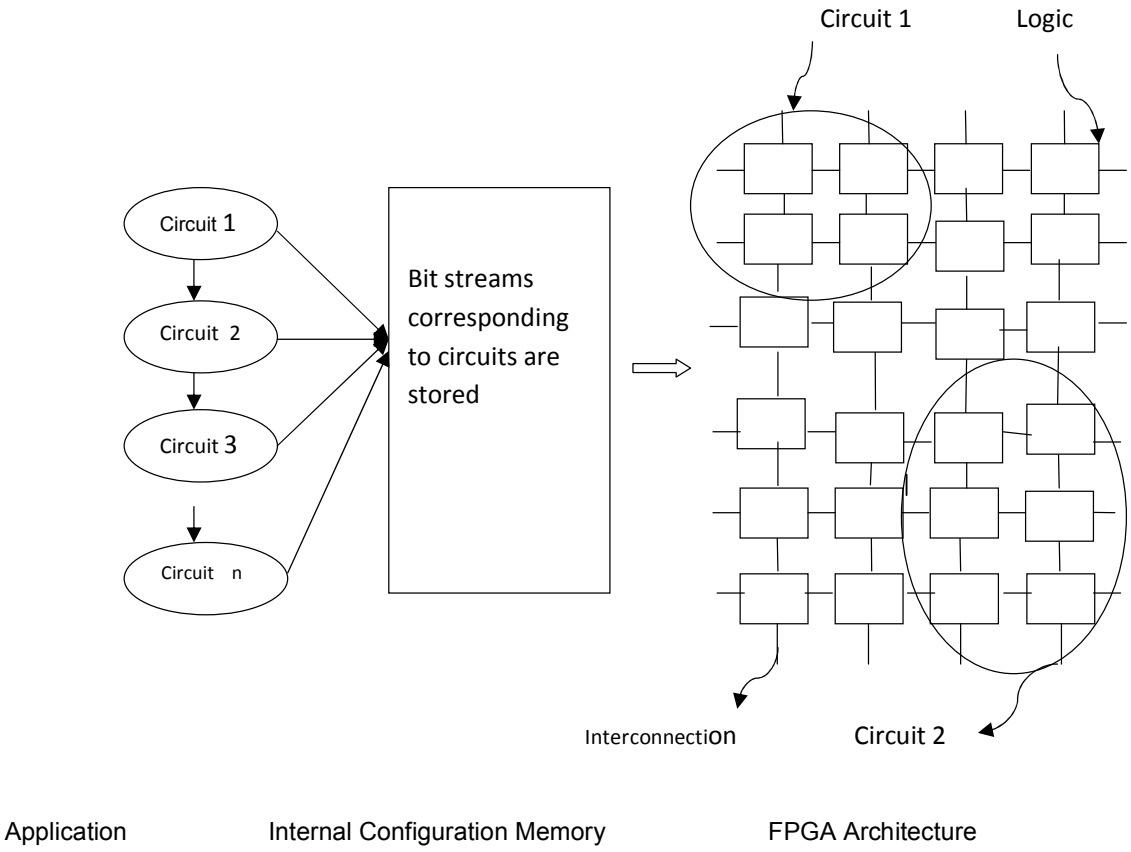

Figure.2 Steps involved in Configuration of FPGA for an application

III.a. CLASSIFICATION OF FPGA AND ITS MODEL

Based on mode of configuration, FPGA is classified into two types as static and dynamic. Reconfiguration of FPGA by not interrupting current execution of application is called as static reconfiguration. But by interrupting the small portion of current running application, updating the configuration of FPGA dynamically is called as dynamic reconfiguration. Selective updating of logic blocks and its interconnections is otherwise called as run time partial reconfiguration (. e.g., Virtex II, Virtex II Pro, Virtex-4, Virtex-5 , ATMEL etc, from XIlinx).Xilinx XC6200 Series, Virtex series, Atmel AT4000 and AT6000 Series are Dynamic FPGA's.

Table.1. Types of FPGA's and its versions and models.

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Types of FPGA	Definition	Versions
Static	Updating the configuration without interrupting the current running application execution.	Virtex-II,Virtex II Pro, Virtex -4, Virtex-5, XCV2000E- Partially Reconfigurable FPGAs
Dynamic	Updating the configuration by interrupting the current running application execution.	XC6200 Series, Atmel AT 4000, AT 6000-dynamic Reconfigurable FPGAs

Total FPGA Area is denoted as wxh, where 'w' denotes the width and 'h' denotes the height. In 2D FPGAs, task can be placed anywhere, suffers from both internal and external fragmentation.In 1D FPGAs, the columns are fixed, tasks can be placed anywhere along the horizontal direction. It suffers from internal fragmentation. In homogeneous FPGA, the array is full of logic blocks and interconnections, but in heterogeneous FPGA, in addition to logic blocks, it has few dedicated in-built blocks such as BRAM's , DSP processors and Embedded Memories, Current field of research in reconfigurable systems focus on developing integrated partitioning, Scheduling and placement algorithms for 1D heterogeneous FPGAs in applications such as embedded computing, neural networking, image processing etc.,.

IV. RECONFIGURATION OVERHEAD

The performance improvement in dynamic reconfigurable computing systems is degraded by an demerit factor called reconfiguration overhead. It is nothing but the number of times the FPGA is reconfigured and also it directly affects the on-line scheduling and placement of hardware tasks. Since the reconfiguration is unavoidable, developing the efficient scheduling and placement algorithms to reduce the reconfiguration overhead is the major issue. On-going research works deals with developing online scheduling and placement algorithms to reduce the reconfiguration overhead in run time partial reconfiguration FPGAs. Elena perez-ramo et al. [9] proposed the survey of various techniques to reduce the reconfiguration overhead. Tom Degryse et al. [43] developed the loop transformation method to reduce the overhead with matrix multiplication as an example.

Ali ahmadinia and Jurgen Teich [3] developed an new fitting algorithm to reduce the reconfiguration overhead in turn speed up the online placement for FPGAs. Elena perez Ramo et al. [8] proposed the configuration memory hierarchy that provides the first Reconfigurable Computing system with energy savings of 22.5%,without performance degradation by developing the configuration mapping algorithm and integrated into reconfiguration computing manager. Farhad Mehdi pour et al. [10] concentrating on reducing the Reconfiguration latency that affects the system performance and develop temporal partitioning algorithm. For set of data flow graphs, the placement time improvement range from 0% to 37.5% and reconfiguration speed improvement range from 0.0 to 1.24.

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Javier Resano et al. [16] discuss the specific scheduling support to reduce the reconfiguration overhead especially for embedded applications and the result shows the 93% reduction in overhead from the initial overhead. Configuration reusing and configuration prefetching are the two methods proposed by Javier Resano etal [17] to reduce the overhead and the improvement factor is by 4. Javier Resano et al. [18] developed the hybrid design time/runtime prefetch heuristic to reduce the reconfiguration overhead and the result shows the overhead reduced by 5% to 93%.

Sungjoon Jung et al. [38] proposed the resource sharing algorithm exploiting the static partial reconfiguration to reduce the overhead and the result shows that the algorithm sharing is of 6.82% and reusing resources of 80.8%. Rahul Kalra and Roman Lyseeky [33] addressed the relationship between the several hardware task scheduling algorithms and their impact on the number of reconfigurations required to execute. Some replacement policies like Random, Least recently used, most recently used, low-priority based scheduling policies are introduced to improve the placement by using these policies to schedule the real time tasks in embedded applications. On average, the LPTL reduce the number of reconfigurations by 21% as compared to random schedulers.

V. TASK MODEL AND SURVEY OF SCHEDULING AND PLACEMENT PROBLEMS AND ITS ALGORITHMS

V a. TASK MODEL

Definition: Task is defined as the function synthesised to digital circuit and programmed into Reconfigurable computing Device. It has size and shape. The following table .2 tabulates the task model and its definitions.

Table.2 Task Model

S.no	Task Factors	Definition
1	Task Size	Defines the area requirement in FPGA

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2	Task shape	Mostly Rectangular shape
3	Task denotion	Ti= { wi,hi,ei,ai,di,ri} where wi= width , hi-height, ei=execution time, ai=arrival time di-deadline (for real time tasks) ri=reconfiguration time
4	Task Classification	Real time/non real time (soft/ hard), dependent/ independent
5	Task execution	Preemptive/ Non pre-emptive

V b. SURVEY OF ALGORITHMS FOR SCHEDULING AND PLACEMENT OF HARDWARE TASKS IN RECONFIGURABLE COMPUTING SYSTEMS

System performance in terms of speed and energy consumption completely depends on how fast the hardware tasks are scheduled and placed inside the FPGA area. Scheduling defines the time instant at which task has to start its execution. Scheduling methods are developed with resource constraints or time constraints. Referring, Sahib H.Gerez [35] the types of scheduling and its constraints are tabulated in table.3

Table.3 Classification of Scheduling and its constraints

Classification of scheduling	Constraints
As-soon-as Possible (ASAP) scheduling	Time Constrained
As late as Possible (ALAP) scheduling	Time Constrained
Force Directed scheduling	Time Constrained
List based Scheduling	Priority based, Resource constrained
Freedom based/ mobility based scheduling	Time constrained/ Resource constrained
Simulated annealing/ Path based scheduling	Time constrained/ Resource constrained

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Michael C.Farland et al. [30] addressed the high level synthesis definition and its importance in computer aided design of VLSI circuits and issues in high level synthesis. Xue-jie zhang et al. [45] discussed the importance of scheduling process in high level synthesis and the work is carried out using genetic algorithm.

***Survey of partitioning methods**:* FPGA with limited resources cannot occupy the large applications, so partition the input application into various circuits of small size that too fit inside FPGA area. Partitioned circuits exploit more parallelism and it will be of either spatial or temporal. This section deals with survey of few partitioning methods. Abelardo Jara-Berrocal et al. [1] proposed temporal partitioning method in which time multiplexing the available hardware resources for large applications is carried out and the performance is improved by 44%. Yan bing Li et al. [46] proposed recurrent structures based task partitioning using new graph theoretical algorithm. Mustafa Imran Ali [31] deals with integrated temporal partitioning and scheduling process. In mind with reducing the reconfiguration latency, K.S.Chatta et al. [22] developed the fine grained hardware/software partitioning algorithms. Since most of the research work concentrates on homogeneous FPGA, the partitioning algorithm for heterogeneous FPGAs is developed by Sudharsan Banerjee et al. [37].

***Survey of Scheduling and Placement Methods**:* As reconfiguration overhead directly affects the reconfigurable computing system performance, most of the research work concentrates on reducing it by developing the efficient scheduling and placement algorithms. The following section deals with survey of few scheduling and placement algorithms and its performance. Maisam mansub basssiri et al. [26] developed the configuration reusing based on-line scheduling algorithm to reduce the overhead and also the task rejection rate is reduced. Zhiyuan Li et al. [47] concentrated on reducing the reconfiguration latency by exploring various configuration prefetching techniques and the performance is increased by factor of 2. Due to high computation time of evolutionary algorithms based scheduling, it's not suitable for online large applications. Christopher Steiger et al. [6] proposed new non-preemptive scheduling techniques named as horizon and stuffing and the performance improvement from 1d to 2D is 75% -98%. Ali Ahmadinia et al. [2] suggested a new online hardware task dynamic scheduling and placement method and the work is experimented on 2D CLB array of Xilinx XC 2000-E device, cluster based method is used to improve the placement performance by 20% and task rejection rate is 16.2%.

Thomas Marconi et al. [41] proposed an intelligent stuffing method is used to improve the quality of placement and the performance results is shown as 89.75 reduction in total wasted area, 1.5% in scheduling time and 31.3 % shorter response time and is suitable for embedded applications. Jin Cui et al. [20] proposed an one-level look a head optimization algorithm to improve the on-line placement and reduce the fragmentation for aperiodic soft real time tasks. Klaus Danne et al. [25] developed an algorithm for pre-emptive execution of periodic real time tasks named as EDF-NF and MSDL (Merge server distribute load). The performance result shows EDF-NF outscripts the MSDL in scheduling performance, task utilization factor is around 85% and task acceptance is 75%.Thomas Marconi et al. [39] presented the novel configuration circuit to speed up the reconfiguration and relocation for partially reconfigurable devices.

Helbert walder et al. [13] developed the algorithm for the placement of non-rectangular based on best-fit and footprint transform which results less fragmentation and the performance result shows the execution time increased by 8.7%. Christoph steiger et al. [5] developed the fast on-line placement and guarantee based

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scheduling algorithms based on small task first and EDF (earliest deadline first) concept]. Helbert walder et al. [14] developed the online scheduling algorithms for block partitioned devices based on shortest remaining processing time (SRPT) and EDF (earliest deadline first) concept.

Frank Vlaardingerbroek et al. [11] developed the scheduling and defragmentation algorithms for heterogeneous FPGAs scheduling algorithms developed are FCFS(First come First serve), SJF (shortest job first), Smallest Job First(SJF) . Jin Cui et al. [21] proposed an efficient algorithm named Scan line algorithm (SLA), for online management of PR-FPGA where the concept of finding the complete set of Maximum set of rectangles for on-line scheduling and placement of hardware tasks is used. Thomas Marconi et al. [42] proposed the various intelligent merging techniques for on-line placement in Partially reconfigurable Computing systems and the performance result shows that comparing to to Bazargan's algorithm, the placement quality is improved by 1.72 times. Kiarash Bazargan et al. [24] discussed the various fast placement algorithms and the experimentation is carried out. Philip Mahr et al. [32] discussed the integrated temporal partitioning, module selector and placement of tasks for dynamic network on chip and evaluate the performance. S.Roman et al. [34] proposed the algorithms for scheduling of multitasks in heterogeneous FPGAs and its performance is evaluated by considering set of data flow graphs. Thomas Marconi et al. [40] focused on developing the online hardware task scheduling and placement on 3D Partially reconfigurable FPGAs.

Fragmentation defined as the partition in area of FPGA during the placement of hardware tasks, is an serious issue. The current research work in reconfigurable computing focussed on developing the defragmentation algorithm in addition to scheduling and placement algorithm .To reduce the fragmentation in placement of tasks , the re-location of modules approach is applied, especially for heterogeneous FPGAs. Sandar P.Fekete et al. [36] proposed an dynamic defragmentation algorithm for 1D heterogeneous FPGAs, the performance result shows that maximal free space to locate the new arriving tasks is increased by 30%. Manuel G.Gericota et al. [27] and Markue Koester et al.[29] addressed the defragmentation issue for heterogeneous FPGAs. Jesus Tabreo et al. [19] addressed the defragmentation measures for reconfigurable systems management. J.Septien et al. [15] proposed the perimeter quadrature based metric is used to measure the fragmentation. Trong-yen Lee et al. [44] developed the algorithm for on-line free space management of online placement for reconfigurable systems.

VI. CONCLUSION

To satisfy the demand of high performance computing in applications of embedded computing, image processing and cryptography, reconfigurable computing platform should be designed with the excellent operation system. On-line Scheduling and placement of hardware tasks in both real time and non-real time are critical issue in designing operating system for reconfigurable computing platforms. This paper deals with the comprehensive knowledge of such scheduling and placement algorithms and their simulation performance.

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